An Ultra-Wideband Common Gate LNA With Gm-Boosted And Noise Canceling Techniques

Amin Jamalkhah*
Department of Electrical Engineering, Shahid Bahonor University of Kerman, Kerman, Iran
a.jamalkhah@eng.uk.ac.ir
Ahmad Hakimi
Department of Electrical Engineering, Shahid Bahonor University of Kerman, Kerman, Iran
hakimi@uk.ac.ir

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Abstract
In this paper, an ultra-wideband (UWB) common gate low-noise amplifier (LNA) with g_m-boosted and noise-cancelling techniques is presented. In this scheme we utilize g_m-boosted stage for cancelling the noise of matching device. The bandwidth extension and flat gain are achieved by using of series and shunt peaking techniques. Simulated in .13 um Cmos technology, the proposed LNA achieved 2.38-3.4dB NF and S11 less than -11dB in the 3.1-10.6 GHz band. Maximum power gain (S21) is 11dB and -3dB bandwidth is 1 .25-11.33 GHz. The power consumption of LNA is 5.8mW.

Keywords: G_m-Boosted, Low Noise Amplifier, Noise- Cancelling, Ultra-Wideband, Shunt and Series Peaking.

1. Introduction

In recent years, the demand for ultra-wide band systems has increased. These systems are a new wireless technology, which have the ability to send data over a wide spectrum of frequency bands [1]. The advantages of this technology include high data rate, low power, reduced interference and low-cost, that are critical for broadband wireless communication. An UWB LNA is a first block in an ultra-wide band transceiver and Its performance can affect the overall performance of the transceiver. The UWB LNA must be able to provide several basic requirements, such as broadband input matching, low noise figure (NF), sufficient gain to reduce the noise of the mixer, small die area and low power consumption.

Several techniques have been reported in published literature to design UWB LNAs with high performance. Based on the characteristics of the noise and input matching, the UWB LNA can be divided into two main groups, the common gate (CG) LNA, and the common source (CS) [2], [3]. Although the noise figure of CG LNA is more than CS configuration, but the low input impedance of CG LNA in a wide spectrum of frequency band, makes it attractive for LNA design. Thus, the common gate LNA is suitable to achieve broadband input matching [2]. The noise figure of the CG LNA $(1+\gamma/\alpha)$ [4], depends on the process parameters and device size, and almost remains constant with frequency. Also, the NF and input impedance of the CG LNA have a tight relationship with each other. To avoid tight relationship between the input resistance and the noise figure of the CG LNA, we can use g_m-boosting technique [5]. Also to release this trade-off in the CG LNAs a noise-cancelling technique [6] has been widely used. From a feed-forward path the noise of the CG transistor is reduced, while the input impedance is matched simultaneously.

In this work we will combine these two techniques. The g_m-boosting stage made with a common source amplifier. In order to cancel the noise of CG transistor, instead of using feed-forward path, we utilize g_m-boosting stage to cancel the noise of the input matching transistor. However this technique needs extra PDC budget for g_m-boosting stage, in general the total power consumption is low and NF will improve. For achieving the bandwidth extension and flat gain, we use shunt-series peaking and stagger compensation techniques [7]. In section II the proposed LNA and considerations of it will be described. The simulation results are presented in section III.

2. Proposed UWB CG LNA With g_m Boosted and Noise Cancelling Techniques

2.1 Basic idea

The principle of noise canceling is to generate the noise signals with the opposite phase polarities in different paths and adding them at the output. The conceptual diagram of the proposed technique is shown in Fig.1. This LNA is composed of a transistor M_1, two auxiliary amplifiers (A_1 and A_2), and R_s is source impedance. Thermal noise of the matching device M_1, $I_{n,M1}$, generates a voltage noise at node x. A_1 act as g_m-boosting stage and the generated noise voltage at node x, amplified by a factor of $-A_1$ and applied to node y.

The noise current due to the channel of M_1 (I_1) goes to the output. For canceling the noise of M_1, the voltage noise in node *y* must be converted to current noise with the opposite phase polarity to the polarity of I_1. Therefore

* Corresponding Author

to generate such current, an auxiliary amplifier is required. A_2 act as an auxiliary amplifier and convert the voltage noise in node *y* to current noise (I_2). For canceling the noise of the input transistor M_1, I_1 and I_2 must be equal with the opposite phase polarities. A_1 and A_2 in addition to canceling the noise of the M_1, increase the effective transconductance and the total gain of the LNA will be increased. In summary the combination of A_1 and A_2 provide another current path, which result in reduced noise and increased overall gain. The noise canceling condition is as below

$$A_1 A_2 R_s = 1 \quad (1)$$

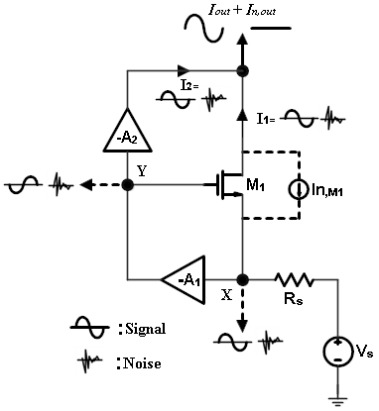

Fig. 1. Conceptual diagram of the proposed LNA with g_m-boosted and noise-canceling techniques

As shown in (1), A_1 and A_2 are inversely related to each other, and the power consumption of LNA will be reduced.

The proposed LNA is shown in Fig. 2. The "main CG amplifier", made with M_1 and R_1, is enhanced by the "A_1" made with M_2 and R_2. M_3 act as A_2. According to voltage noise in node y, We need a CS configuration (M_3) to eliminate the noise of the input matching device. M_4 and M_5 act as a highly linear output voltage buffer. The output buffer is used to drive a 50-Ω load for simulation results. L_0 provides Biasing of M_1 and also resonate with input parasitic capacitance to provide wideband input matching. In order to achieve an UWB LNA, we utilize $L_{1\text{-}3}$ for bandwidth extension and flat gain (shut-series peaking techniques) [7]. All of inductors are on chip with low Q. $C_{0\text{-}4}$ are coupling capacitors.

The noise canceling condition is as below

$$g_{m2} g_{m3} R_2 R_s = 1 \quad (2)$$

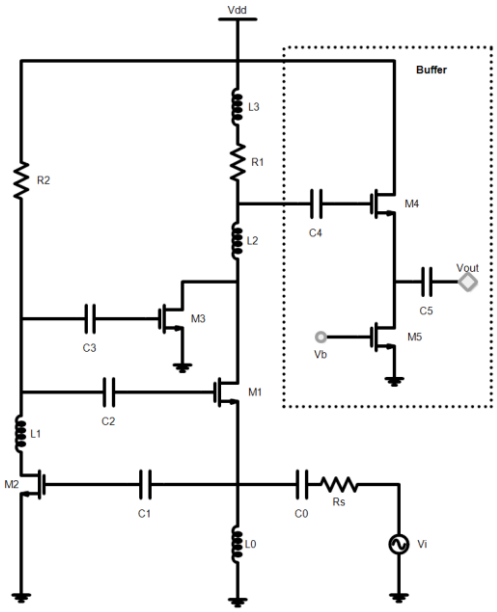

Fig. 2. Complete circuit schematic of the proposed UWB LNA with the output buffer.

2.2 Input matching

G_m-boosted technique employs feed-forward to avoid tight relationship between the input resistance and the noise figure [8]. As shown in Fig.1, for an input voltage change of ΔV, the gate-source voltage changes by -(1+A)ΔV and the drain current by -(1+A)g_m ΔV. Thus the g_m increased by a factor of 1+A1 [8]. By using this technique the input impedance of the proposed UWB LNA is as below

$$Z_{in} = \frac{1}{g_{m1}(1+A_1)} \| sL_0 \| \frac{1}{sC_{in}} \quad (3)$$

Where $A_1=g_{m2}R_2$ and C_{in} is the total parasitic capacitance at the input. By increasing the operating frequency of the circuit, the parasitic input capacitance C_{in} starts playing critical roles, and performance of the LNA at high frequencies reduced. For the UWB LNA, S11<-10dB is needed from 3.1–10.6 GHz. With proper selection of L_0 and C_{in} values, the parasitic capacitance C_{in} absorbed by L_0 and the imaginary part of Z_{in} is negligible within the bandwidth. A low quality factor (Q) for the input matching network suggest a possible broadband impedance match.[9]

2.3 Gain and bandwidth

The effective transconductance of proposed LNA is as below

$$G_{m,eff} = (g_{m1}(1+g_{m2}R_2) + g_{m2}g_{m3}R_2)/2 \quad (4)$$

Under input-impedance-matching and noise canceling conditions, the effective transconductance become $1/R_s$. As frequency increases, the parasitic capacitances at the nodes of the circuit, reduce the gain and bandwidth of the circuit. One way to increase the bandwidth is utilizing shunt and series peaking techniques [7]. In shunt peaking

technique an inductor (L_3) connected in series to the load to broaden the bandwidth. In nodes with significant parasitic capacitance, the series peaking technique can be used. In these nodes, an inductor ($L_{1,2}$) is inserted to separate total capacitance into two constituent capacitance. By inserting the inductor, a peaking will be created above the -3db frequency and then by compensating this peaking, larger bandwidth will be achievable. To reduce peaking in the frequency response and in order to broadens the magnitude response, we utilize $L_{1,2}$ with low quality factor [7]. At the resonance frequency of the input matching network (ω_0), the input matching is the best and degrades on the either side, because the quality factor (Q) of the matching network in the input is low. When the load is resistive, for a broadband response there is a significant roll-off in the transconductance gain after ω_0. By using this roll-off, canceling the peaking due to series peaking technique in the transimpedance gain at the output and flatten the overall gain of the amplifier will be achieved. This is done through proper staggering of the resonance frequencies of input matching and series peaking technique [7].

2.4 Noise analysis

The dominant noise source in a common-gate LNA, is channel noise of the input matching transistor, which is equal to ($\gamma/\alpha g_m R_s$), where γ and α are the process dependent parameters. The g_m can be increased to reduce the noise, since the noise and input matching of the CG stage are inextricably related, increasing the g_m degrades the input matching. In order to avoid tight relationship between the noise figure and input matching, we use g_m-boosted and noise canceling techniques together. Also the effective transconductance increased, which result in increased gain and reduced NF. In order to simplify the calculation, it is assumed that the output impedance of transistors is infinite and input bias current is ideal. Furthermore only the thermal noise of the channel transistors and resistors are considered. The noise factor F (NF=10logF) can be derived from

$$F = \frac{V^2_{n,out}}{4KTR_S A_V^2} = \frac{I^2_{n,out}}{4KTR_S G_m^2} \quad (5)$$

$I_{n,out}^2$ and $V_{n,out}^2$ are the output current and voltage noise, A_v^2 and G_m^2 are the voltage gain and transconductance under input-impedance-matching and noise canceling conditions. The low frequency noise factor components can be derived as

$$F_{M2} = \frac{\frac{\gamma}{\alpha} g_{m2}(g_{m3}R_2)^2}{R_S G_m^2} = \frac{\gamma}{\alpha} \times \frac{1}{R_S g_{m2}} \quad (6)$$

$$F_{M3} = \frac{\frac{\gamma}{\alpha} g_{m3}}{R_S G_m^2} = \frac{\gamma}{\alpha} \times \frac{1}{g_{m2} R_2} \quad (7)$$

$$F_{R2} = \frac{R_2 g_{m3}^2}{R_S G_m^2} = \frac{1}{g_{m2}^2 R_2 R_S} \quad (8)$$

$$F_{R2} = \frac{1}{R_1 R_S G_m^2} = \frac{R_S}{R_1} \quad (9)$$

The noise due to terms (6-8) are inversely related to g_{m2}, so g_{m2} can be increased to lowering the total NF. By increasing the g_{m2}, to establish input impedance matching and noise canceling conditions, g_{m1} and g_{m3} must be reduced, therefore the power consumption of the $M_{1,3}$ will be reduced. For large g_{m2}, the width of M_2 must be increased. However, this increases the parasitic capacitances in drain and gate of M_2, deteriorating the gain and NF at high frequencies. Also due to the effect of parasitic capacitance in the drain of M_3, the gain decrease, and the NF will be increased at higher frequencies. To mitigate these effects and increasing the bandwidth, series peaking inductors ($L_{1,2}$) insert to these nodes. Fig.4 show the NF and power gain (S21) with and without the inductors L_1 and L_2. Without L_1 and L_2, NF and gain of the LNA degrade at high frequencies.L_1 and L_2, lowering the effects of parasitic capacitances of the circuit at high frequencies, and result in improved NF and gain at high frequencies. Also the effective transconductance $G_{m,eff}$ in the input matching and the noise cancelling conditions, become $1/R_s$, compared to conventional CG LNA is higher and NF will be reduced. However large g_{m2}, requires an extra PDC budget, but the total power consumption of LNA is low.

2.5 Process variations

Inter-die and intra-die variations are two sources of variations in CMOS technologies [10]. Inter-die variation is typically accounted in circuit design as a shift in the mean of some parameter ("e.g.,V_{th} , μ_n ,.."") equally across all devices or structures on any one chip. This type of variation can be compensated by proper biasing of the circuit [11]. Intra-die variation (mismatching) is the deviation occurring spatially within any one die that can be solved by layout techniques and proper sizing. In this work we focus on the inter-die variations.

Inter-die variations modeled as worst case process corners. In CMOS manufacturing process there are five process corners (TT, FF, SS, FS, SF). For instance in fast corner, all process variation deviate toward a device with increase current, threshold voltage V_{th} and gate oxide thickness T_{ox} decrease and mobility μ_n increase. Fig .3 shows the constant bias scheme that used in the circuit to reduce the effect of inter-die variations.

Threshold voltage variation has a greater impact on the drain current, thus the effect of V_{th} variations on V_b will be studied. In fast corner V_{th} decrease and result in increase drain current (I_d), voltage drop across R increased and V_b will be reduced. The following expressions are achieved from [10].

$$v_b = V_{dd} - R\ I_d \quad (10)$$

$$I_d = K'(V_b - V_{th})^2 \quad (11)$$

where k'=(1/2)($\mu_n C_{ox}$W/L) is the transistor parameter. By combining of (10) and (11), V_b can be derived as

$$V_b = V_{th} + \frac{\sqrt{2\ K'R\ (V_{dd} - V_{th}) + 1} - 1}{K'R} \quad (12)$$

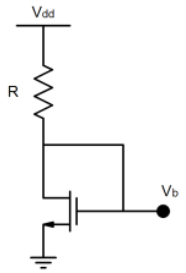

Fig.3. Bias network

V_{th} variation result in V_b variation as follows

$$\delta V_b = \frac{\partial V_b}{\partial V_{th}} \partial V_{th}$$

$$= \delta V_{th} - \frac{\delta V_{th}}{\sqrt{2\ K'R\ (V_{dd} - V_{th}) + 1}} \quad (13)$$

In (13) by choosing a large R the second term will be negligible and V_b variation will be approximately equal to the V_{th} variation "i.e., the decreases in the V_{th}, will decreases the voltage bias V_b and vice versa." As mentioned before, in inter-die variation all devices suffer from same variation on the chip. The drain current "$I_d=k(V_b-V_{th})^2$" of the transistors which are biased with the constant bias circuit (Fig.3), almost remains unchanged against the V_{th} variations. Thus LNA works properly in different process corner.

3. Simulation Results

The LNA is simulated by Advanced Designed System (ADS) in 0.13um CMOS. Figures 5-7, show the S11, power gain (s21), and NF of LNA at different process corners respectively. Since the circuit has only NMOS transistors, only three corners are shown. The S11 is shown in Fig.5 and is less than -11 dB at 3.1-10.6 GHz band in different corners. L_0 and C_{in} resonate with each other to provide wideband input matching. Also we cannot choose large L_1, because L_1 affects on the input matching, thus the value of L_1 is selected so that the input matching of the circuit remains below than -10dB in the bandwidth of the circuit. Fig.6 shows S21 of the LNA at different process corners. In TT, FF, and SS corners, maximum power gain (S21) achieved at 5 GHz, 5.4 GHz and 4.75 GHz respectively which is 11.6dB, 12.5dB, and 10dB respectively. The -3dB bandwidth is 10.46 GHz (1.2 to 11.66 GHz) in TT corner, 11 GHz (1 to 12 GHz) in FF corner, and 9.76 GHz (1.1 to 10.86 GHz) in SS corner. The NF of the LNA is lower than 3.7dB in TT corner, 3.4 dB in FF corner, and 4.5dB in SS corner from 3.1-10.6 GHz and is shown in Fig.7. Minimum NF of LNA in TT, FF, and SS corners respectively is 2.48 dB at 5.44 GHz, 2.31 dB at 5.5 GHz and 2.7 dB at 5.3 GHz. Simulating of IIP3 is done by Two-tone test with 10 MHz spacing, which is shown in Fig.8. At 6GHz, the simulated IIP3 is -13 dBm.1dB compression gain is -25 dBm (fig.9).

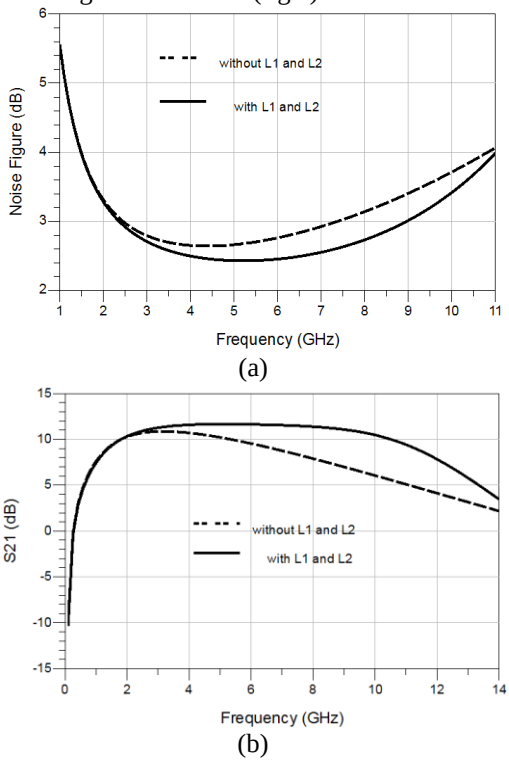

Fig. 4. NF and Power Gain (S21) with and without inductors L1 and L2

Table 1. COMPARISON WITH UWB CMOS LNAs

Process	-3dB Band [GHz]	NF [dB]	S11* [dB]	S21* [dB]	S12* [dB]	P1dB [dBm]	PDC [mW]	Vdd [V]	Circuit Topology	Reference
0.18µm	3.1-10.6	4.5-6.2	-9.5	13.2	n.a.	-11	28	1.8	CG+ double resonant load	[12]
0.18µm	1.5-11.7	3.74-4.74	-8.6	12.26	-26	-22	10.34	1.8	Current-reuse technique	[13]
0.18µm	.5-11	3.9-4.5	-9	10.2	n.a.	n.a.	14.4	n.a.	Dual-channel shunt technique	[14]
0.18µm	3-10.35	3.3-11.4	-8.3	12.5	n.a.	-14	7.2	1.2	CG+ resonant load	[15]
0.18µm	1.2-11.9	4-5-5.1**	-11	9.7	-35	-16	20	1.8	Broadband noise-cancelling	[16]
0.13µm	**1.25-11.34**	**2.38-3.4****	**-11**	**11**	**-35**	**-25**	**5.8**	**1.2**	**G_m-boosted+noise cancelling techniques**	**This work**

*Maximum values,**In the 3.1-10.6 GHz band.

The power consumption of the LNA is 4.14mW without the output buffer and 5.8mW with the output buffer. Table I shows the comparison of this work with the previous published UWB LNAs.

4. Conclusions

An UWB CG low noise amplifier (LNA) based on G_m-boosted and noise-cancelling techniques, was presented. By using these two techniques low NF achieved. By employing an inductor with low Q in the input of LNA, broadband impedance match achieved. The bandwidth of LNA improved by utilizing series and shunt peaking techniques. By using stagger compensation technique flat gain over the bandwidth achieved. By utilizing the constant bias circuit, LNA worked properly in different process corners. Simulation results for the proposed LNA realized in 0.13um CMOS demonstrate 11-dB maximum power gain, 2.38-dB minimum NF while dissipating 4.85mA from 1.2-V supply.

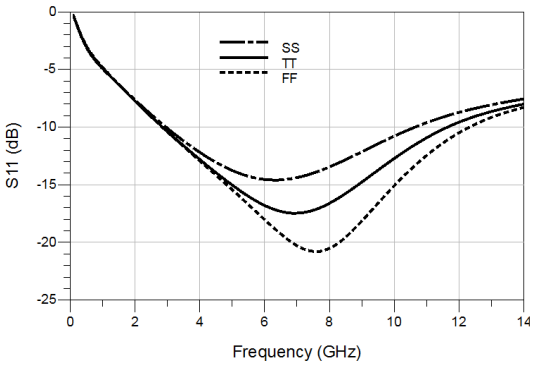

Fig. 5. S11 at different process corners

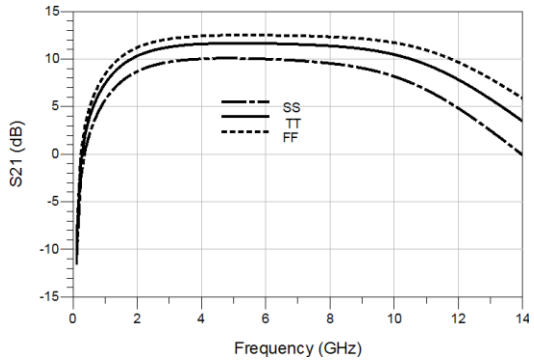

Fig. 6. S21 at different process corners

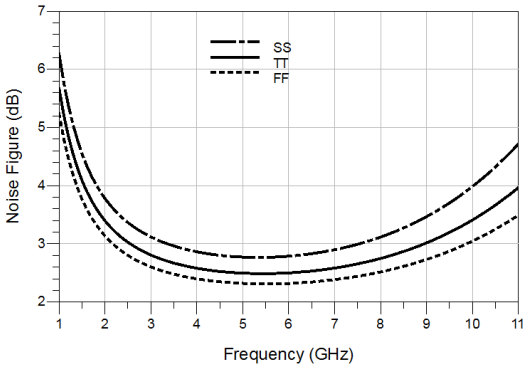

Fig. 7. NF at different process corners

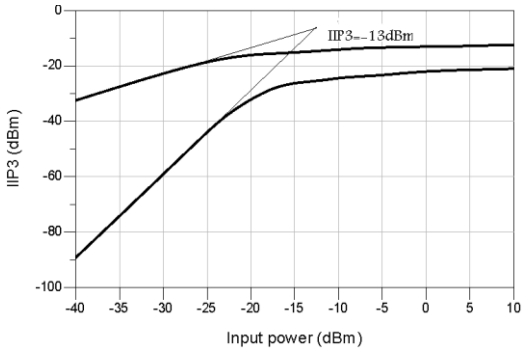

Fig. 8. IIP3 of the LNA at 6 GHz

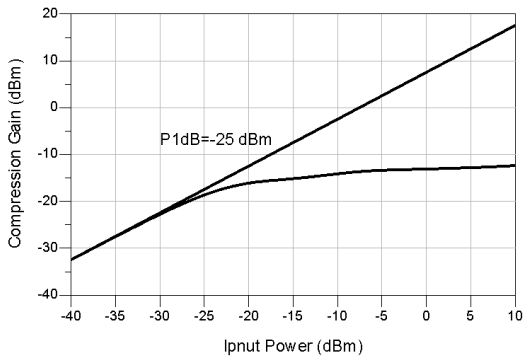

Fig. 9. 1dB Compression point

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Amin Jamalkhah received the B.Sc. degree in electrical engineering from Lorestan University, Khoramabad, Iran in 2011, and M.Sc. degree in electrical engineering from Shahid Bahonar University of Kerman,Iran in 2014.His general research interests include CMOS RF circuits for wireless communications.

Ahmad Hakimi received the Ph.D. degree from the Istanbul Technical University. His research interests are analog CMOS integrated circuit design, nonlinear circuit theory and applications, RF microelectronics.