

# A Low-Jitter 20-110MHz DLL Based on a Simple PD and Common-Mode Voltage Level Corrected Differential Delay Elements

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## Abstract

In this paper, a 16-phases 20MHz to 110MHz low jitter delay locked loop, DLL, is proposed in a 0.35 $\mu$ m CMOS process. A sensitive open loop phase detector, PD, is introduced based on a novel idea to simply detect small phase differences between reference clock and generated delayed signals. High sensitivity, besides the simplicity reduces the dead zone of PD and gives a better jitter on output generated clock signals, consequently. A new strategy of common mode setting is utilized on differential delay elements which no longer introduce extra parasitics on output nodes and brings the duty cycle of generated clock signals near to 50 percent. Also, small amplitude differential clock is carefully transferred inside the circuit to considerably suppress the noise effect of supply voltage. Post-Layout simulation results confirm the RMS jitter of less than 6.7ps at 20MHz and 2ps at 100MHz input clock frequency when the 3.3Volts supply voltage is subject to 75mVolts peak-to-peak noise disturbances. Total power consumption reaches from 7.5mW to 16.5mW when the operating frequency increases from 20MHz to 100MHz. The proposed low-jitter DLL can be implemented in small active area, around 380 $\mu$ m $\times$ 210 $\mu$ m including the clock generation circuit, which is proper to be repeatedly used inside the chip.

**Keywords:** Delay Locked Loop; Clock Generation; Low-Jitter Clock Distribution; Wide-Range DLL; Low-Jitter DLL.

## 1. Introduction

Delay locked loops, DLLs, are broadly used for low-jitter multiphase clock generation, [1], [2] and [3]. Multiple operations within multitask mixed signal applications are regularly scheduled using a digital switching strategy on a single hardware. Recently, for example, single-stage analog comparators are proposed to perform three operations (reset, pre-amplification and latch) in a single hardware, [6], [7] and [8]. Also, the switching strategy of sample and holds (S/H) in high speed and high resolution analog to digital converters (ADCs) should be strictly considered to meet the desired resolution and jitter specifications through sampling. In low jitter applications, although PLLs can considerably reject the input clock jitter due to generating a fresh and low jitter clock by the VCO, however, smaller area and lower power consumption introduce DLLs as a proper choice when they are repeatedly used inside the chip. Furthermore, PLLs are regularly used for generation of very high frequency clock signals due to the inherent abilities of ring and LC oscillators. Whereas, DLLs are usually utilized to generate multiple phases of a middle

frequency reference clock signal, manually generated inside or transferred into the chip.

Frequency-Phase detectors (Phase Detectors), PFDs (PDs), are known as the main building blocks of PLLs (DLLs), [10], which dominantly determine the sensitivity of closed loop structure. Reducing the dead-zone of PD dominantly improves the RMS and peak-to-peak jitter of DLL because this makes the loop to response to small phase differences. Hence, employing a sensitive PD is one of the main challenges of DLL design. This is highlighted when DLL is used in jitter sensitive applications, such as high resolution ADCs, when the RMS jitter of generated clock directly affects the dynamic behavior, (e.g., SNDR). The conventional phase detectors, [2] and [5], are constructed from positive feedback NAND gates which opposes against changing stored values on output nodes. Hence, larger phase differences are required at PD's inputs to firstly remove the previous data and secondly develop the new charge on output nodes of PD. This means larger dead zone and smaller sensitivity. Also, non-differential or pseudo-differential delay cells are applied in [2] and [5], in which the power supply noise can directly emerge on generated clocks and consequently diminish the RMS jitter.

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In this paper, a low jitter DLL is proposed based on fully differential delay cells to considerably alleviate the supply noise on output generated clocks. A sensitive PD is introduced in section II to reduce the jitter besides the simplicity. Compatible charge pump and delay cells are also proposed in this section. Moreover, a simple strategy of common mode (CM) level setting is proposed to bring the generated phases around the middle point of supply and ground voltages. This CM setting strategy, no longer introduces extra parasitic capacitances on the output nodes of delay elements, and yields a better duty cycle, near 50 percent, when the outputs of delay elements are used via simple inverters. The strategy of transferring small signal input clock and generating full range reference clock inside the chip is discussed in section III. The duty cycle adjuster circuits, as used in [4], are not required when the combination of CM setting strategy and clock transferring is applied. Simulation results are shown in section IV and finally, section V concludes the paper.

## 2. Building Blocks of the Proposed DLL

Building blocks of the proposed DLL are illustrated in Fig.1. Eight differential delay elements are employed to provide 16-phases. Input reference clock and its complementary, Clk and Clkb, are applied to a PD as reference clocks. Also, the 180° delayed clock, Clk<sub>180°</sub>, which is generated on one of the output nodes of delay cells, is fed back to PD to form the close loop structure of DLL. PD produces a digital pulse with the width of phase difference between digital inputs. Namely, generated pulse of PD is modulated with the phase difference. An analog charge pump is required to translate the generated digital pulse to analog control voltage, V<sub>C</sub>, to be prepared for the next use by delay cells.

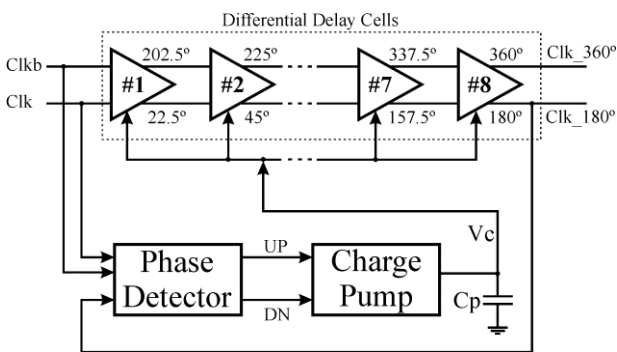


Fig. 1. Block Diagram of the Proposed DLL

V<sub>C</sub> adjusts the delay of cells in close loop structure in such a way that no phase difference is remained on inputs of PD. Hence, 360° phase difference is expected through the cells. Propagating the same delays, 16 phases should be produced in 8 differential elements which means 22.5° phase shift between generated clocks in current and neighbor cells. To produce similar signal transitions on generated phases, equal capacitive loads are considered for all cells. Hence, dummy loads are required for other phases when Clk<sub>180°</sub> is reused by PD.

### 2.1 Phase detector

The proposed phase detector is shown in Fig.2(a). Unlike the other similar works, three digital input signals are here used to detect the phase difference. PD can be divided into two main sections: the main core of phase detection which generates Q<sub>2</sub>, and the pulse generator logic which provides UP and DN signals. As depicted in Fig.2(a), the main core of PD is constructed from two clocked inverters employed in master-slave configuration. Namely, Clk<sub>180°</sub> is applied as input signal of a master-slave clocked buffer which is controlled by differential reference clocks, called Clk and Clkb. When the falling edge of Clk arrives before/after the falling edge of Clk<sub>180°</sub>, high/low level of input voltage would be buffered to node Q<sub>2</sub>. Signal transitions are also clarified in Fig.2(b).

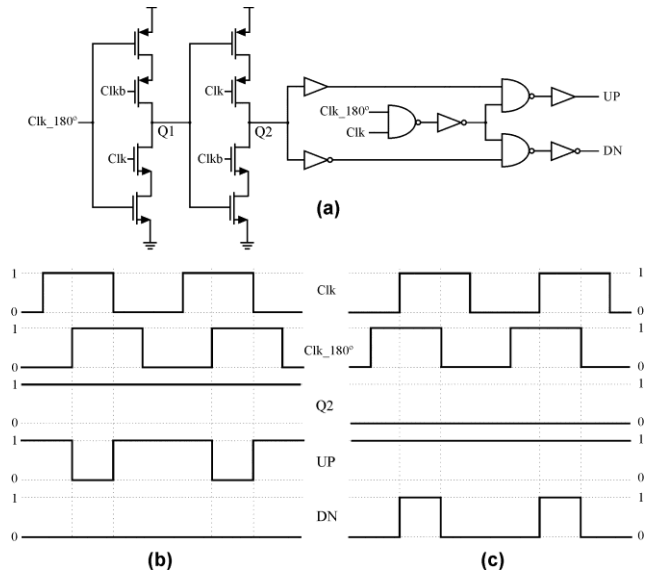


Fig. 2. (a) The Proposed Phase Detector, The Case of (b) Increasing and (c) Decreasing Delay

Hereafter, pulse generator generates narrow pulses of up and down operations. When Q<sub>2</sub> is set to high level voltage, pulls DN down to zero and produces the inverted overlap of Clk and Clk<sub>180°</sub> at UP node. In the other case, as depicted in Fig.2(c), when Q<sub>2</sub> goes down to zero value, pulls the UP node up and produces the overlap of Clk and Clk<sub>180°</sub> at DN output. The sensitivity of the proposed PD is only restricted by the required time for sampling in master clocked inverter as introduced as the main core in PD. In the other works, [2] and [5], where positive feedback structure is used for phase detection, a time portion should be allocated to overcome the positive feedback and remove the previous latched data.

### 2.2 Charge pump

The schematic of the compatible charge pump is illustrated in Fig.3 which provides the analog voltage based on generated pulses of PD, UP and DN. M<sub>p2</sub> and M<sub>n2</sub> are controlled by UP and DN signals. Detail description of charge pump behavior can be separately

surveyed for two cases of Fig.2(b) and 2(c). In the case (b), when the DN signal is set to zero, the discharge direction is closed and falling edges of UP signal opens the charge direction of the load capacitance through  $M_{p1}$  and  $M_{p2}$ . In the other case, when the falling edge of  $Clk_{180^\circ}$  occurs before the falling edge of the sampling clock, Fig.2(b), UP goes up to high level voltage which disconnect the charging direction of the load capacitance. Furthermore, DN represents the overlap of  $Clk$  and  $Clk_{180^\circ}$  which discharges the  $V_C$  via  $M_{n1}$  and  $M_{n2}$  when goes to high level. Decreasing  $V_C$  speeds up the delay elements.

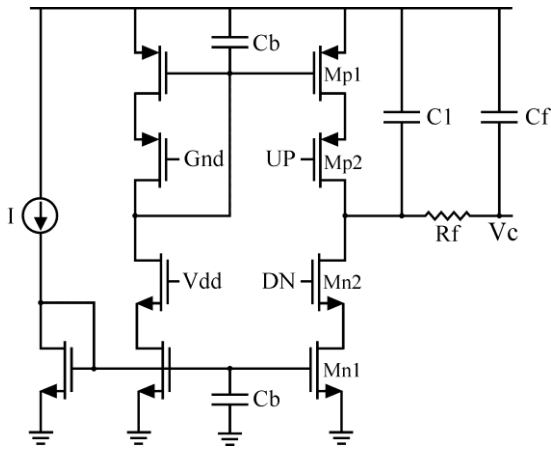


Fig. 3. Compatible Charge Pump and Low Pass Filter

### 2.3 Differential delay elements

Detail description of differential delay cells is shown in Fig.4 in which  $V_C$  determines the bias current. As depicted in Fig.4, increasing  $V_C$  slows down the delay elements due to decreasing the bias current. Bias adjusting is continued until the falling edge of reference Clock,  $Clk$ , corresponds on rising edge of  $Clk_{180^\circ}$ , which means  $180^\circ$  phase shift. Due to the differential structure of delay elements in Fig.4,  $360^\circ$  phase shift is expected from  $Clk$  to  $Clk_{360^\circ}$ . Differential structure of delay cells might encounter the problem of mismatch between up and down tail current sources. This might shift up or down the cross points of differential delayed signals from the middle of supply and ground voltages. If the outputs of delay elements are applied on inverter gates to drive other loads, the cross point should be adjusted near the threshold of a simple inverter gate. Otherwise, the duty cycle undesirably deviates from 50 percent at outputs of inverter gates. Hence, an internal feedback is required to adjust the cross points by compensating up and down tail current sources. The main concern of using regular common mode setting strategies is reducing the upper limit of operating speed due to introducing capacitive loads on output differential nodes. A new CM setting strategy is proposed which no longer introduce extra capacitive loads on output nodes. On the other hand, sensing the average value of differential outputs from output nodes of delay cells slows down the transitions of delayed clocks due to introducing extra parasitics. This

effect could be considered as an offset delay which restricts the speed of DLL.

Since the differential outputs of each cell are applied as the inputs of the next one, cross level is emerged on the average value of nodes X and Y due to the source follower combination of input devices in differential pair. Hence, the DC-level of each stage is sensed at the next one via two resistors,  $R_{CM}$ , and then is corrected by changing the up and down tail currents via  $M_{CMP}$  and  $M_{CMN}$ , as depicted in Fig.4. This means a simple averaging on generated clock signals without reducing speed. Considering a larger value for  $R_{CM}$ , however, a portion of tail current of differential pairs is inevitably used for CM level setting.  $M_{BN}$  and  $M_{BP}$  are employed to enhance the resolution of current mirror by providing the similar conditions for both bias and tail current sources.

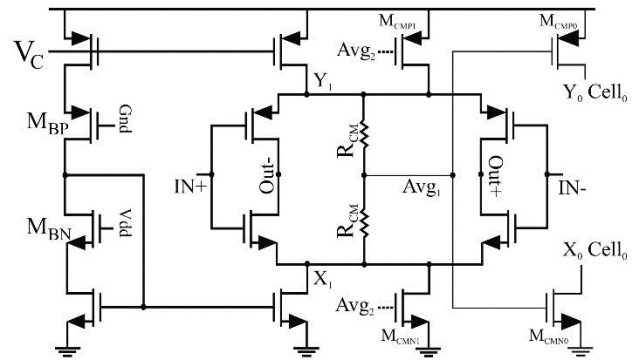


Fig. 4. Differential Delay Elements and DC-Level Setting Strategy

### 3. Generating Low-Jitter Reference Clock

Reference differential clocks, should be carefully transferred inside the chip. Hence, the circuit of Fig.5 is employed to alleviate the supply noise and generate low jitter reference clock.  $Ck$  and  $Ckb$  represent the smaller amplitude clock signals which should be transferred inside the chip and generate full range reference clocks,  $Clk$  and  $Clkb$ . The simple circuit of Fig.5(a) produces the filtered supply and ground,  $V_{dd\_FLTR}$  and  $Gnd\_FLTR$ , from noisy supply.  $M_1$  and  $M_2$  are NMOS and PMOS transistors which are selected in large size to play the role of low pass filter's capacitance along with  $R_1$ . The voltage drop across  $R_1$  depends on the current drawn by the next devices which introduces a constraint on selecting  $R_1$  value.  $M_3$  and  $M_4$  generate the threshold voltage of a simple inverter, TH, which is around the middle point of the differential supply range when  $M_3$  and  $M_4$  are properly scaled. Threshold voltages of the same size inverter gates are approximated to be identically varied at several corners. Hence, TH is also affected as the same as the threshold voltage of inverter gates at several corners to eliminate the dependency of the duty cycle to corner variations. This fact is here considered by generating TH through  $M_3$  and  $M_4$  and using as reference voltage. Hence, the duty cycle adjuster circuits, as used in [4], are not

required. As shown in Fig.5(b), a simple differential pair is applied to amplify the small amplitude of input differential clock around the DC-level which is set to threshold voltage of an inverter gate.  $M_5$  and  $M_6$  are also used as resistors to complete the DC-level setting strategy. Here, the filtered supply and ground are used as the differential supply of differential pair and inverters. Clk and Clkb are low jitter and full range reference clock signals which are generated in a reasonable duty cycle.

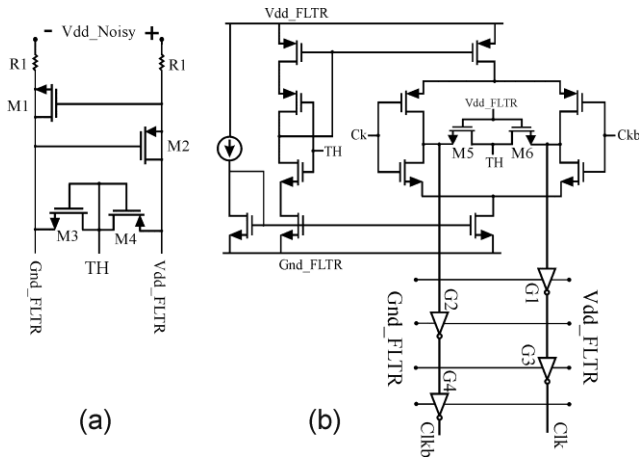


Fig. 5. Low-Jitter Reference Clock Generation via (a) Filtered Supply and Corner-Dependent Reference Generation, and (b) Full Range Recovery Circuit

### 4. Post-Layout Simulation Results

Layout pattern of the proposed DLL in a 0.35 $\mu$ m CMOS technology is illustrated in Fig.6 which confirms that the proposed 16-phases DLL could be implemented in about 380 $\mu$ m $\times$ 210 $\mu$ m active area. The layout pattern of Fig.6 also includes the clock generator circuit of Fig.5.



Fig. 6. Layout Pattern of the Proposed DLL

Post-layout simulations of the proposed DLL are performed for the range of 20MHz to 110MHz operating frequencies. A peak-to-peak power supply noise of around 75mv is also constructed by a set of sinusoidal waveforms with different amplitudes and frequencies. Larger values of noise components are assigned to the amplitudes of the multiples of input clock frequency, to highlight the noise of clock coupling on the power supply lines. For example, amplitude of around 16mv, 10mv and 15mv are considered

for 20MHz, 40MHz and 60MHz frequencies, when the DLL is simulated at 20MHz. The noisy and the filtered supply of Fig.5(a) are illustrated in Fig.7(a) and 7(b). Settling behavior of the control voltage,  $V_C$ , is also depicted in Fig.7(c) at 20MHz operating frequency.

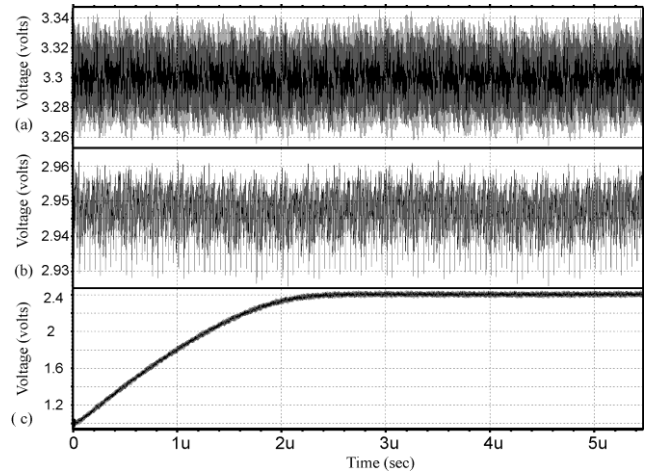


Fig. 7. (a) Noisy and (b) Filtered Vdd, (c) Control Voltage at 20MHz

After settling, 16 phases are generated through 8 differential delay cells as depicted in Fig.8 in which the delay time of generated phases differs from the neighbor one, equal to 1/16 of the period time of the reference clock. The generated phases at 20MHz are illustrated in Fig.8. which all are differed 22.5 degrees from each other.

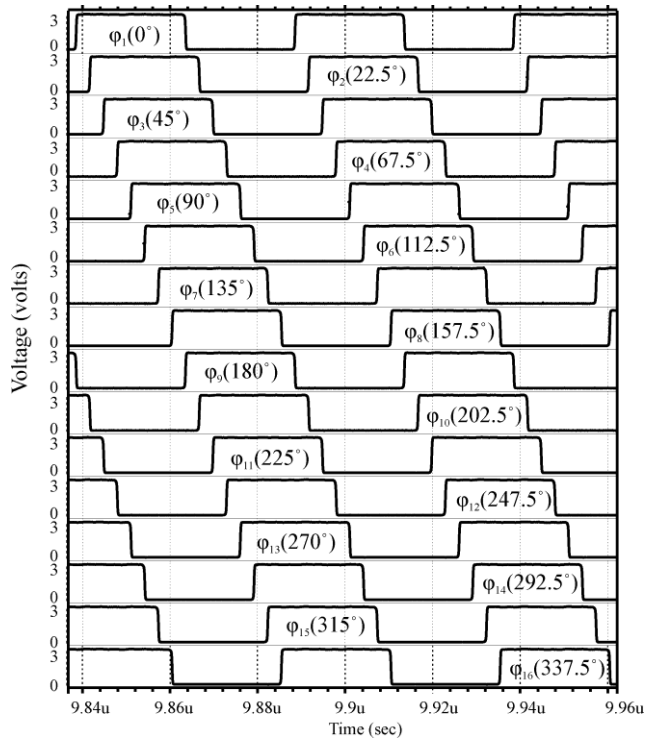


Fig. 8. All Generated Phases at 20MHz Operating Frequency

Settling behavior of  $V_C$  is also shown in Fig.9 at 100MHz operating frequency. As discussed earlier,  $V_C$  is expected to settle to smaller values when the operating frequency is increased.

Input clock jitter would not be eliminated in DLL's output, meanwhile, PLLs can suppress the input clock jitter due to providing a new and fresh clock on VCO's output. Firstly, a low-jitter input clock signal is utilized as reference clock to qualify the jitter of the proposed DLL when supply is subject to around 75mv peak-to-peak noise. Noise harmonics are manually weighted at multiples of the fundamental clock frequency as expected in real test conditions. Firstly, the circuit of Fig.5(b) is simulated to qualify the jitter behavior of full-range clock inside the chip, in presence of 75mv peak-to-peak noise on supply voltage. The eye diagram of small amplitude clock, ck and ckb, and generated full range signals, clk and clk, are illustrated in Fig.10 at 100MHz input clock frequency, when the supply voltage is subject to 75mv peak-to-peak noise. Jitter histogram of the generated full-range clock is also illustrated in which the peak-to-peak and RMS jitter of 10.4ps and 2.1ps are obtained, respectively.

Eye diagram and jitter histogram is evaluated for one of outputs at 100MHz operating frequency. Results are illustrated in Fig.11 which shows around 11ps peak-to-peak and RMS jitter, respectively. Simple comparison between reference clock and generated outputs, clarifies that the RMS jitter of input clock would be similarly emerges on outputs in DLL loop structure.

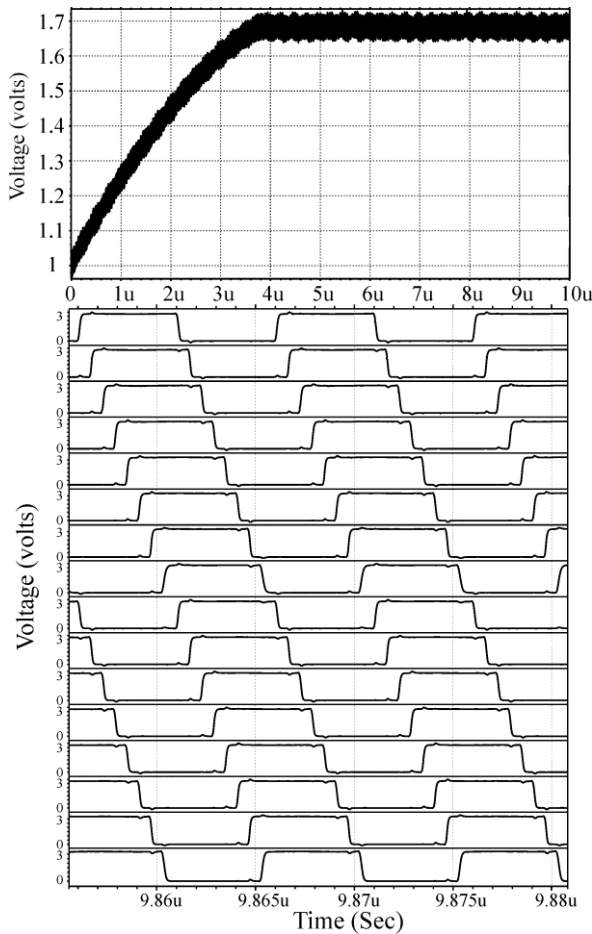


Fig. 9. The Control Voltage and Generated Phases at 100MHz

To evaluate this claim, a manual peak-to-peak jitter of around 2.3ns is applied on reference input clock which represents the RMS jitter of around 58ps on small amplitude reference signals. As illustrated in Fig. 11 peak-to-peak jitter of output generated clock is similarly increased when the reference clock is encountered to jitter disturbances. Hence, suppressing the supply noise is the main challenge of designing low-jitter DLLs.

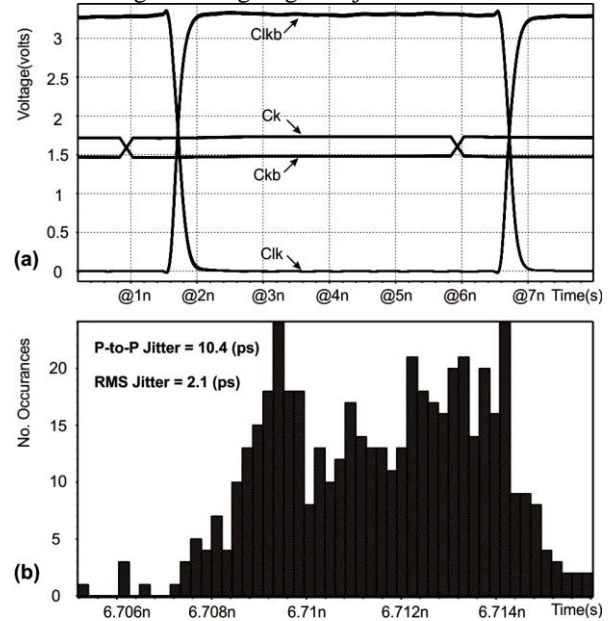


Fig. 10. (a) Eye diagram of Small Amplitude Input and Generated Full-Range Reference Clock (b) Jitter Histogram of Full-Range Reference Clock. @100MHz in Presence of 75mv Peak-to-Peak Supply Noise

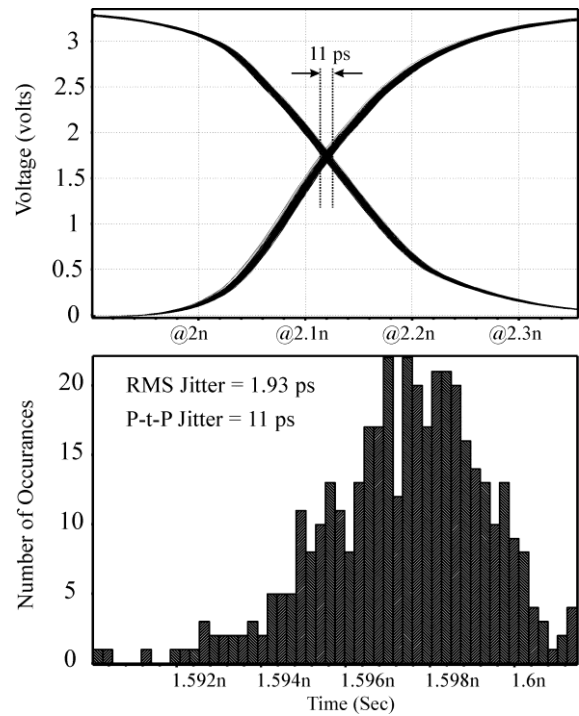


Fig. 11 Eye Diagram and Jitter Histogram of Differential Output Clocks at 100MHz Operating Frequency in Presence of 75mv peak-to-peak Supply Noise

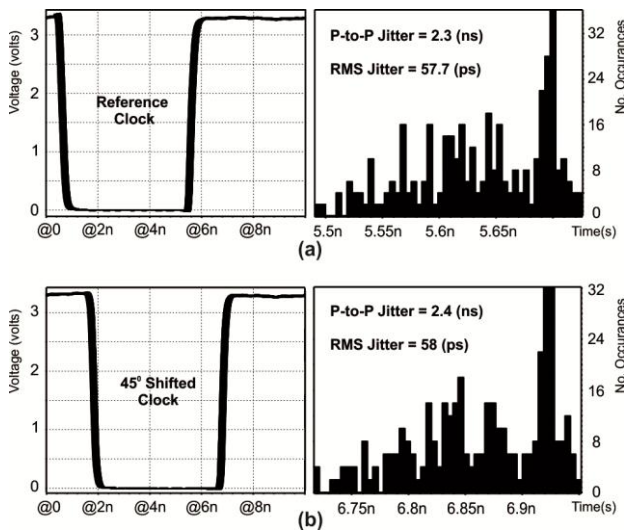


Fig. 12. Eye Diagram and Jitter Histogram of (a) Input Jittery Reference Clock (b) 45° Generated Clock, in Presence of 75mv Peak-to-Peak Supply Noise and 2.3ns Peak-to-Peak Jitter on Input Reference Clock

Table 1 summarizes the DLL specifications for 20MHz, 50MHz, 80MHz and 100MHz operating frequencies when the supply is subject to 75mv peak-to-peak noise. As shown, the value of  $V_C$  is decreased for higher operating frequencies.

Table 1. DLL Specifications at Different Operating Frequencies

	20 MHz	50 MHz	80 MHz	100 MHz
RMS Jitter (ps) @ 75mv p-t-p Supply Noise	6.7	5	4.5	2
Power Consumption (mW)	7.6	10.5	14.2	16.5
Control Voltage, $V_C$ (volts)	2.4	2.1	1.85	1.45

## References

- [1] X. Gao and et Al., "Advantages of Shift Registers Over DLLs for Flexible Low Jitter Multiphase Clock Generation", IEEE Transaction on Circuits and Systems-II, Vol. 55, No. 3, March 2008.
- [2] D. J. Foley and et Al., "CMOS DLL-Based 2-V 3.2-ps Jitter 1-GHz Clock Synthesizer and Temperature Compensated Tunable Oscillator", IEEE Journal of Solid-State Circuits, Vol. 36, No. 3, March 2001.
- [3] G. Dehng and et Al., "Clock-Deskew Buffer Using a SAR-Controlled Delay-Locked Loop", IEEE Journal of Solid-State Circuits, Vol. 35, No. 8, August 2000.
- [4] Y. Jung and et Al., "A Dual-Loop Delay-Locked Loop Using Multiple Voltage-Controlled Delay Lines", IEEE Journal of Solid-State Circuits, Vol. 36, No. 5, May 2001.
- [5] J. Kim and et Al., "A Low-Jitter Mixed-Mode DLL for High-Speed DRAM Applications", IEEE Journal of Solid-State Circuits, Vol.35, No.10, October 2000.
- [6] S. Kazeminia, M. Mousazadeh, Kh. Hadidi and A. Khoei, "High-speed low-power Single-Stage latched-comparator with improved gain and kickback noise rejection", IEEE Asia Pacific Conference on Circuits and Systems, APCCAS 2010. Page(s): 216 – 219
- [7] S. Kazeminia, M. Mousazadeh, Kh. Hadidi and A. Khoei, "A 500MS/s 600 $\mu$ W 300 $\mu$ m<sup>2</sup> Single-Stage Gain-Improved and Kickback Noise Rejected Comparator in 0.35 $\mu$ m 3.3v CMOS Process", IEICE Transactions on Electronics, Vol. E94.C, No. 4, April 2011, pp. 635-640
- [8] S. Kazeminia, O. Shino, E. Haghghi and Kh. Hadidi, "Improved Single-Stage Kickback-Rejected Comparator for High Speed and Low Noise Flash ADCs", 21th European Conference on Circuit Theory and Design, ECCTD 2013, Accepted and will be published on Sep. 2013.
- [9] S. Kazeminia, Kh. Hadidi, A. Khoei, "A Low Jitter 110MHz 16-Phase Delay Locked Loop Based on a Simple and Sensitive Phase Detector", 21th Iranian Conference on Electrical Engineering, ICEE, May 2013.
- [10] B. Razavi, "Design of Analog CMOS Integrated Circuits", Boston, MA: McGraw-Hill, 2001, Chapter 11, pp: 377-389.

## 5. Conclusions

A low-jitter 20MHz-110MHz DLL is proposed based on a simple and sensitive open loop phase detector. Also, a simple strategy of cross couple setting is introduced on differential outputs to provide 50% duty cycle digital signals. Hence, the duty cycle adjustment block is not required. The strategy of transferring low-noise reference clock signals inside the chip has been also discussed.

Table 2 compares the proposed DLL with other similar works. Small Active area and power consumption, introduces the proposed DLL as a proper choice when the DLL should be repeatedly used inside a chip. Furthermore, the maximum operating frequency is reversely proportional to the number of delay cells in closed loop structure. Namely, smaller delay values are expected from each delay cell, when the loop is constructed from further number of delay elements in similar conditions. Hence, the maximum operating frequency is reduced in this work.

Table 2. Comparison Table

	[2]	[4]	[5]	This work
Process ( $\mu$ m)	0.5	0.25	0.6	0.35
Maximum Operating Frequency (GHz)	1	0.4	0.22	0.11
Supply (volts)	2	2.5	3.3	3.3
No. Phases	9	8	15	16
PtP Jitter (ps) @ Supply Noise	20 N.A	54 Quiet	49 N.A	11 @75mv
RMS Jitter (ps) @ Supply Noise	3.2 N.A	6.7 Quiet	6.4 N.A	2 @75mv
Power(mW)	33	60	33	16.5
Area (mm <sup>2</sup> )	0.6	0.13	0.45	0.08

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