

# A 2-bit Full Comparator Design with a Minimum Quantum Cost Function in Quantum-Dot Cellular Automata

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## Abstract

In recent years, reduction of the complementary metal-oxide-semiconductor (CMOS) circuit's feature size has posed significant challenges, such as current loss and leakage and high power consumption. Consequently, further size reduction of CMOS technology is not feasible. As an emerging nanoscale technology, quantum-dot cellular automata (QCA) can be utilized in the near future for designing computers and very-large-scale integration (VLSI) circuits. QCA technology makes it possible to design low-power, high-performance, and area-efficient logical circuits. A comparator function is a digital logical function which compares and evaluates whether or not a bit is greater than, smaller than or equal to the other bit (half comparator). A full comparator has a third input which shows the result of the previous step. Half and full comparators play an essential role in CPU architecture. The current paper proposes a full comparator circuit based on QCA and a new quantum cost function. In addition, a 2-bit comparator is presented based on the introduced full comparator. Employing the new quantum cost function, the present study compares the proposed full comparator design with previously presented designs in terms of area, delay, and complexity. Comparisons show that the proposed design occupy less area and produces less delay and so is more suitable for usage in CPU design.

**Keywords:** Quantum-Dot Cellular Automata; Full Comparator; Cost Function; QCA Cell; Majority Gate; NOT Gate.

## 1. Introduction

In recent years, complementary metal-oxide-semiconductor (CMOS) technology has encountered different challenges, such as high power consumption and current leakage. Minimizing CMOS circuits involves particular problems, including the occurrence of various physical phenomena, namely a particular mass of each element and quantum effects, all of which pose obstacles to proper operation of transistors. Consequently, researchers are seeking smaller technologies with lower power consumption and less current leakage [1-3].

Quantum-dot cellular automata (QCA) is considered to be among the six emerging technologies with higher performance. Even though QCA circuits are associated with more challenges than are faced by CMOS, the simple structure of QCA circuits has led researchers to further study their implementation. With its low-power, high-performance, and area-efficiency features, QCA technology can redesign fundamental circuits, such as comparators. As a result, the circuit industry is impacted by the need to propose chip designs that are more practical and provide better performance in QCA technology [4-8].

Section 2 reviews the fundamental blocks in QCA technology and its clocking. Section 3 covers the background of comparators and provides an overview and comparison of QCA designs. Section 4 proposes a 2-bit QCA comparator design while Section 5 introduces a new cost function for the

evaluation of QCA circuits. Based on this cost function, the proposed design is then compared to previous designs.

## 2. Background

This section first provides an overview of the QCA cell structure, QCA wire, and concept of the clock in QCA circuits. The NOT, three-input majority, and five-input majority gates in QCA technology are then introduced.

### 2.1 QCA Cell

In QCA technology, each cell consists of four dots and two electrons which can move freely between the holes or dots. The two electrons have six different states to fill the dots, but not all of these states are stable. The electrons are as far as possible from each other due to Coulomb's repulsive force (i.e., electrostatic gravity and repulsion). As stated earlier, stable states appear when the electrons fill the dots diagonally, which is known as polarization. These two states (Figure 1) demonstrate -1 and +1 polarizations, which are assigned the logical values of 0 and 1, respectively [9,10].

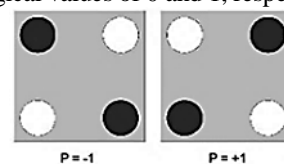


Fig. 1. Two stable states of the basic QCA cell (the cell on the right logical 1; the cell on the left logical 0)

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### 2.2 Wire Structure in QCA

Coulomb’s repulsive force not only works between the electrons in one cell, but it also causes the electrons in each cell to affect the electrons in adjacent cells. The difference between the two is that, when two cells are considered as neighbors, the electrons are placed in a certain state so as to minimize Coulomb’s repulsive force as much as possible. Moreover, an array of lateral cells can be utilized as a wire to propagate information. Figure 2 presents two different models of QCA wires. In the second model (complement chain), the cells are rotated 45 degrees so that the input signal propagates in the odd cells and its complement propagates in the even cells. Placing these two wire models on each other creates a crossing wire model (Figure 3). Due to the difference in cell polarization in the crossing wire model, the two wires do not affect each other [1, 11].

### 2.3 QCA Clock

Because of QCA's structural features, the clock acts as an electronic factor for controlling the movement of electrons within a cell. The clock synchronizes the different parts of the circuit.

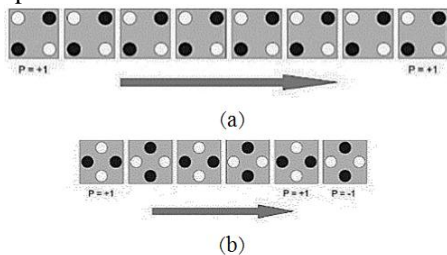


Fig. 2. (a) QCA standard wire, (b) QCA complement wire

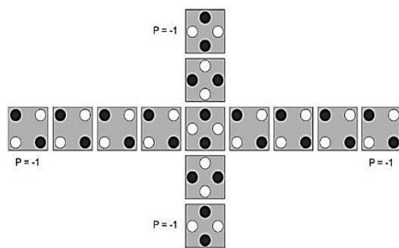


Fig. 3. QCA crossing wire model

Each clock cycle in QCA has four phases (Figure 4): switch, hold, release, and relax. In the switch phase, the polarization of each cell is affected by the adjacent cells. The hold phase places the electrons at the maximum distance from each other so that they enter the stable state. Cells in the hold phase are able to detect the polarization of the adjacent cells in their switch phase. In the release phase, electrons are gradually released and the barrier force declines. In the relax phase, there is no polarization and the electrons may move freely inside a cell [1].

One of the critical issues in QCA clock design is the setting of the four areas in each clock cycle. In fact, misallocation of each clock cycle's areas causes errors in circuit operation. In QCA clock design, coincidences in entering the inputs, wire length, and number of cells in each

phase should be considered. Evidently, data flow control must also be specifically examined in the structural design of QCA and increasing the number of cells in each clock phase achieves this. To prevent noise, a minimum of two cells in each clock phase is necessary. In addition, there should be a threshold value for the maximum number of cells in each clock phase due to the consequences of increasing the number of cells in each phase. Not only does the clock frequency decrease by doing so, but some of the cells may also enter uncertain states due to specified limitations on the energy required to polarize each cell [1,2,8].

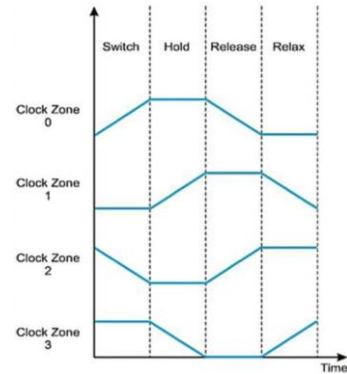


Fig. 4. Clock phase in QCA

### 2.4 Not Gate

The inverter is one of the two fundamental building blocks of each QCA circuit. Figure 5-a presents the basic and simple QCA inverter gate and Figure 5-b provides another NOT gate design, in which the signal enters from the left side and divides into two QCA wires. These signals then merge on the right side. The complement of the entered signal is calculated at the merge time and released on the right side. As a result of Coulomb’s repulsive force in this structure, the stable state of the output is the complement of the input, which thus places the electrons at the maximum distance from each other [1,3,9].

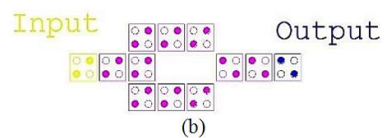
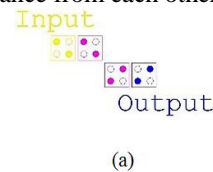


Fig. 5. Two different designs of NOT gate in QCA

### 2.5 Majority Gate

Another fundamental building block of a QCA circuit is the majority gate. Since the majority gate is programmable, it can be used for designing different digital logic structures. As depicted in Figure 6-a, the three-input majority gate has three inputs, an output, and a work cell. The work cell is polarized according to the majority polarizations of the cells, as well as the repulsive force among the three input cells [1].

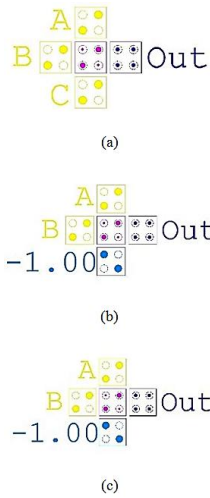


Fig. 6. (a) Three-input majority gate in QCA, (b) Two-input AND gate in QCA, (c) Two-input OR gate in QCA

The logical function of this gate is as follows [1]:

$$M(A, B, C) = AB + AC + BC \tag{1}$$

According to the logical function of the majority gate, if the constant value of -1 (logical zero) is assigned to the C input, it operates as the two-input AND gate (Figure 6-b).

$$M(A, B, 0) = AB + (A)(0) + (B)(0) = AB \tag{2}$$

Moreover, if the constant value of +1 (logical 1) is assigned to the C input, it operates as the two-input OR gate (Figure 6-c).

$$M(A, B, 1) = AB + (A)(1) + (B)(1) = A + B \tag{3}$$

A full comparator design utilizes two different designs of the five-input majority gate. Equation 4 presents the five-input majority gate [1, 14].

$$M(A, B, C, D, E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \tag{4}$$

Figure 7 provides both designs of the five-input majority gate [12, 14].

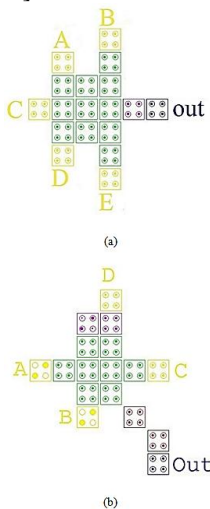


Fig. 7. (a) Five-input majority gate in QCA with 18 cells [15], (b) Five-input majority gate in QCA with 17 cells [12, 13]

As shown in Figure 7-b, A, B, C, and D are the inputs of the gate. In this design, input D acts as two similar inputs. In fact, the two inputs are linked and considered as input D. This majority gate consists of 17 cells [12, 13].

### 3. Comparator Background

Comparators are one of the essential parts of digital logic circuits and have been widely used in CPUs and microcontrollers. Consequently, any progress made in circuit design will improve CPU performance [16-18]. The half-comparator function compares two inputs and produces the result as an output. This output specifies whether a bit is greater than, smaller than or equal to the other bit. Equation (5) depicts the logical function of a half-comparator.

$$\begin{aligned} F_{A>B} &= A\bar{B} \\ F_{A<B} &= \bar{A}B \\ F_{A=B} &= \overline{F_{A>B}} \cdot \overline{F_{A<B}} \end{aligned} \tag{5}$$

where A and B are the inputs and  $F_{A>B}$ ,  $F_{A<B}$ , and  $F_{A=B}$  are the outputs [12]. In full comparators, there is a third input (C) which maintains the result of the previous step at each stage. Equation (6) provides the full comparator functions. Clearly, by assigning a constant value of 1 to input C, the full comparator operates as a half-comparator [12, 16-18].

$$\begin{aligned} F_{A>B} &= A\bar{B}C \\ F_{A<B} &= \bar{A}BC \\ F_{A=B} &= \overline{F_{A>B}} \cdot \overline{F_{A<B}} \end{aligned} \tag{6}$$

In 2008, Y. Xia and K. Qiu proposed the full comparator shown in Figure 8. In this design, a Universal Logic Gate (ULG) is used to build the full comparator and the ULG circuit can operate as any n-input function [15]. With the utilization of ULG, this design exhibits a better performance than that of previous designs employing majority and inverter gates (MI) (Figure 9) [15].

As depicted in Figures 8 and 9, the full comparator design utilizing ULG has fewer crossing wires and its number of cells increased compared to the full comparator design using MI. As a result, circuit performance improved [15].

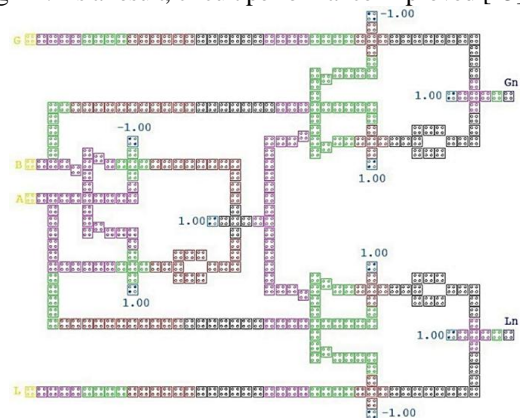


Fig. 8. Full comparator circuit based on QCA utilizing ULG gate [15]

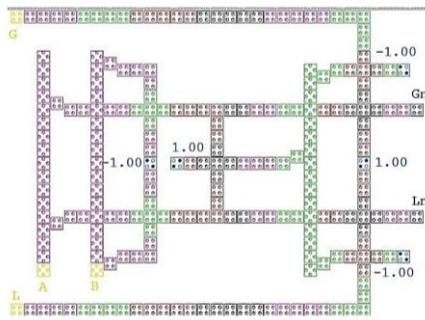


Fig. 9. Design of full comparator in QCA utilizing MI [15]

In 2014, S. S. Anuradha et al. proposed a new full comparator circuit [14]. This circuit introduced a new design for the five-input majority gate (see Figure 7) that was more fault-tolerant in comparison with previous designs. Figure 10 presents the full comparator based on the five-input majority gate. It is notable that the two inputs have a constant value of zero.

As demonstrated in Figure 10, two five-input majority gates and one three-input majority gate were employed in designing this full comparator. There is a significant reduction in the complexity and number of cells in comparison with previous full comparator designs [14].

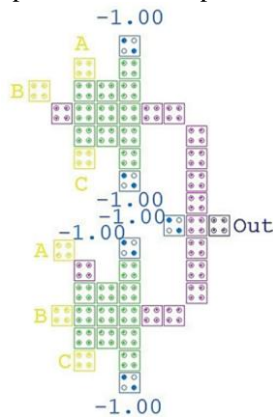


Fig. 10. Full comparator based on the five-input majority

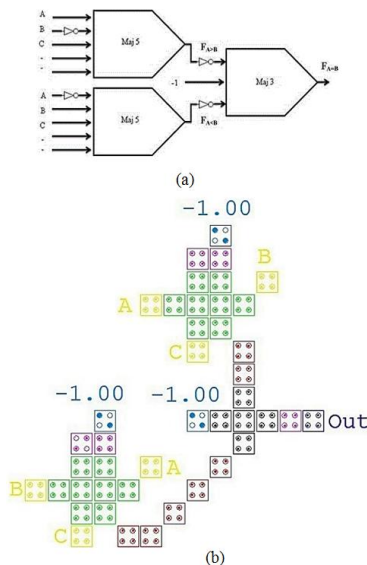


Fig. 11. (a) Schematic (b) Circuit of a full comparator using the five-input majority gate [12]

Figure 11 presents another design for the full comparator with the minimum number of cells in its circuit [12]. This design features the five-input majority gate with 17 cells (Figure 7-b).

This full comparator features two five-input majority gates and one three-input majority. Figure 11-b shows that A and B are the inputs, C is the result of the comparison in the previous stage, and the output is one of three states, namely  $F_{A>B}$ ,  $F_{A<B}$  or  $F_{A=B}$ . Evidently, if input C takes the value of 1, the circuit changes to the half-comparator state. This circuit simultaneously produces two outputs ( $F_{A>B}$  and  $F_{A<B}$ ) and output  $F_{A=B}$  is produced 0.25 clock cycles later [12].

Figure 12 provides the simulation results of the full comparator. According to the simulation, the first two signals represent inputs A and B and the third signal is input C, which is assigned the constant value of zero. In addition, the fourth signal is the output. As shown, the delay of this full comparator is equal to 1.25 clock cycles. In fact, this full comparator has the minimum number of cells as well as less delay in comparison to the other designs.

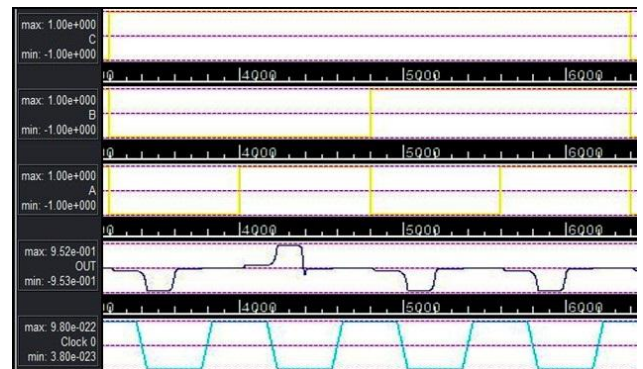


Fig. 12. Simulation of the proposed full comparator using QCA designer software

### 4. Proposed 2-bit Comparator

To compare inputs with a higher number of bits, efficient comparators are needed to evaluate and determine whether the two strings of bits are lower than, greater than, or equal to each other. For this purpose, the present study proposes a 2-bit comparator based on the comparator in [12].

Figure 13 presents the block diagram of the proposed model.

As seen, three 1-bit full comparators compare the two bits. The bits with the same value for each number enter the 1-bit comparators at the same time. Then, in the next stage, the results propagate through the 1-bit full comparator. Figure 14-a and Figure 14-b show the schematic and QCA design respectively. Figure 15 provides the simulation results of the proposed 2-bit comparator. The output of the circuit clearly indicates whether the 2-bit numbers are equal or not. The delay of the proposed circuit is equal to one clock cycle.

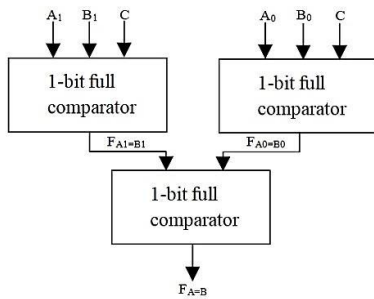


Fig. 13. Block diagram of the proposed 2-bit comparator based on [12]

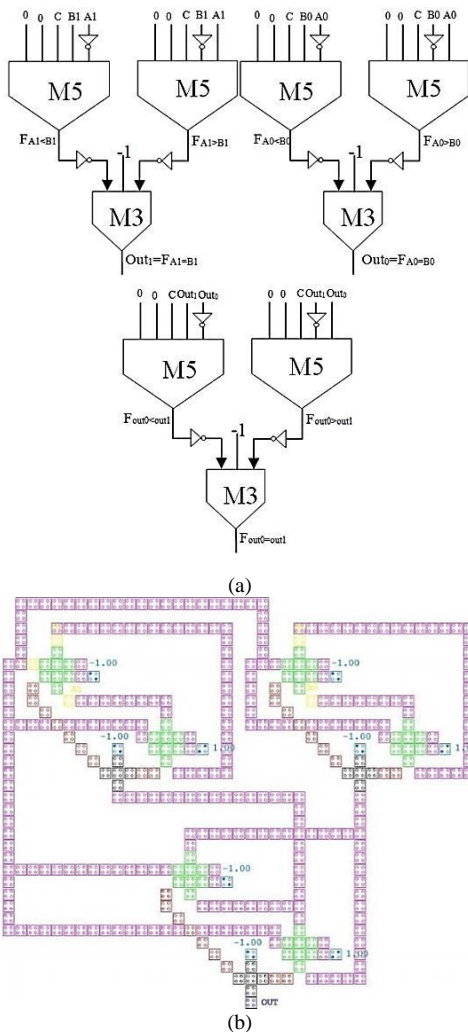


Fig. 14. (a) Schematic (b) QCA design of the proposed 2-bit comparator based on [12]

### 5. Comparison of Full Comparators by the Cost Function

It is very common to introduce a function or an index for evaluating different designs within the same technology as this assists designers to develop better circuits and to compare their design with previous ones [19].

This section proposes a quantum cost function according to QCA features. Then, by the employment of this function, the cost of each full comparator design is calculated.

[17] and [20] introduce a function to evaluate the cost and quality of a QCA circuit. This function shows that the area occupied by a QCA circuit plays a key role in evaluating circuits. One of the advantages of QCA over earlier technologies is its small size. The complexity of a QCA-based circuit is determined based on the number of cells used in the circuit. As the number of cells increase, the polarization of each cell depends on more cells. Furthermore, in most cases, as the number of cells rises, the crossing wires become efficient and so a layered design is beneficial. All of the above points cause the design to occupy more area. The proposed cost function has a direct correlation with the area of a circuit. Another parameter in the evaluation of QCA circuits is power. Lower power is associated with less power dissipation and so it can be claimed that the lower power of QCA circuits produces a better design. Undoubtedly, power has a direct relationship with the cost function as well. Another parameter considered in the evaluation of circuit design is the delay of a circuit. Circuit delay is associated with the complexity of a circuit in certain aspects. Maximum delay occurs when the longest path from the input to the output (i.e., critical path) includes more cells. On the other hand, less delay in the critical path indicates a better design and cost function [17, 20-21].

Equation (7) presents the cost function [21].

$$\text{Cost} = \text{Area} \times \text{Power} \times \text{Delay} \tag{7}$$

Reference [21] indicates that power has a direct and consistent association with complexity.

$$\text{Power} \equiv \text{Complexity} \tag{8}$$

The two parameters affect each other; if complexity increases, power will also grow and vice versa. Overall energy dissipation of a circuit is equal to the amount of dissipated energy in each cell. The energy dissipation of each cell is approximately the same in all cells. Therefore, the amount of energy dissipation in each cell, which is considered to be a constant value for all QCA cells, can be overlooked [17]. To express the overall power consumption in a circuit, the number of cells may be sufficient, eliminating the need to multiply the dissipated energy in each cell by the number of cells [21]. In addition, the power consumption in QCA circuits is so low that it can be ignored.

Thus, another parameter affecting the performance of a QCA circuit can replace that of power. As a result, according to Equation (8), a new cost function is introduced as follows:

$$\text{Cost} = \text{Area} \times \text{Complexity} \times \text{Delay} \tag{9}$$

Therefore, it can be claimed that Equation (9) is another and easier method for correctly evaluating the cost function based on the complexity of a QCA circuit rather than the previously mentioned cost function.

In the following, all the previously full comparators are simulated with QCA Designer software, version 2.0.2, and the cost function is calculated for each of them as well. Moreover, the Bistable simulation engine is employed in the simulation and Table 1 specifies the set values.

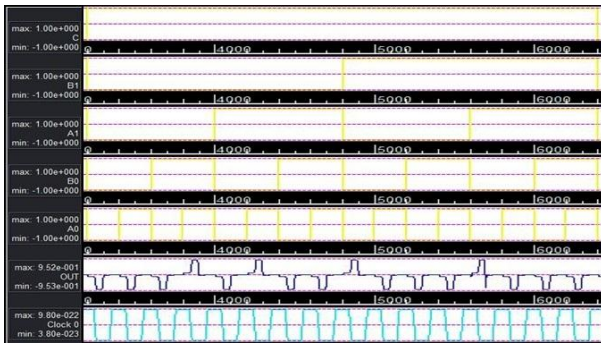


Fig. 15. Simulation of the proposed 2-bit full comparator using QCA designer software

Table 1. Parameters in the QCA Designer Bistable Simulation Engine

Number of Samples	12800
Convergence Tolerance	0.0010
Radius of Effect (nm)	65.0
Relative Permittivity	12.9
Clock High	9.80e-022
Clock Low	3.80e-023
Clock Shift	0.0e+0
Clock Amplitude Factor	2.0
Layer Separation	11.5
Maximum Iterations Per Sample	100
Cell Size (nm)	18×18
Cell Distance (nm)	2
Quantum-Dot Diameter (nm)	5

Table 2 provides the comparison of the full comparator circuits in terms of area, complexity, delay, and cost.

Table 2. Comparison of Full Comparator Circuit Designs

Proposed Design	Area (µm <sup>2</sup> )	Complexity (number of cells)	Delay (clock cycle)	Cost
ULG [15]	0.65	353	2.25	516.2625
MI [15]	0.29	222	2	128.76
Five-input Majority Gate-based Full Comparator [14]	0.09	48	1.25	5.4
Proposed Full Comparator	0.08	43	1.25	4.3

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According to the information in Table 2, there is a significant difference between the full comparator cost introduced in [15] that utilizes ULG and that in [15] using MI. This may be due to the number of cells, as well as the smaller area, when compared to the MI design. Although the delay in [14] and in the proposed design are the same, their area and number of cells differ, thereby resulting in a better cost function. As the cost function considers all the important parameters in QCA-based full comparator designs, it is a favorable benchmark for the comparison of various designs.

### 6. Conclusion

Comparator circuits play a pivotal role in computational operations and are widely used in designing microcontrollers and CPUs. The current paper introduced a full comparator circuit and also presented a cost function to compare the proposed design with other designs. The proposed cost function can serve as a proper benchmark for the overall comparison of different designs. Furthermore, the results of the simulation indicated that the proposed full comparator features the best area and complexity (i.e., number of cells) as well as the best cost value. Therefore, it can be inferred that the introduced full comparator is optimal.

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