A New Calibration Method for SAR Analog-to-Digital Converters Based on All Digital Dithering

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Abstract

In this paper a new digital background calibration method for successive approximation register analog to digital converters is presented. For developing, a perturbation signal is added and also digital offset is injected. One of the main advantages of this work is that it is completely digitally and eliminates the nonlinear errors between analog capacitor and array capacitors due to converter's capacitors mismatch error by correcting the relative weights. Performing of this digital dithering method does not require extra capacitors or double independent converters and it will eliminate mismatches caused by these added elements. Also, No extra calibration overhead for complicated mathematical calculation is needed. It unlike split calibration, does not need two independent converters for production of two specified paths and it just have one capacitor array which makes it possible with simple architecture. Furthermore, to improve DNL and INL and correct the missing code error, sub radix-2 is used in the converter structure. Proposed calibration method is implemented by a 10 bit, 1.87-radix SAR converter. Simulation results with MATLAB software show great improvement in static and dynamic characteristics in applied analog to digital converter after calibration. So, it can be used in calibration of successive approximation register analog to digital converters.

Keywords: SAR; Converter; Calibration; Perturbation; Radix-2; DNL and INL.

1. Introduction

Today, due to the combination of analog and digital integrated circuits, having the appropriate speed and accuracy in data conversion is very important. Hence, successive-approximation-register (SAR) analog-to-digital converters (ADCs) because of establishing a good balance between speed and accuracy as well as lower complexity of circuits than sigma delta converters, flash and other types that either lower speed or accuracy and high circuits complexity and volume, have been considered [1-18]. SAR ADC due to good tradeoffs between speed and accuracy. However, capacitor mismatch in the SAR converters limits the accuracy and resolution of the converter. Commonly, the main factor that limits the linearity in these converters is capacitor mismatch error in digital-to-analog converter (DAC) [10]. Some SAR ADC calibration methods perform the calibration in the analog domain, which requires extra analog circuits [14, 17, 18]. This extra analog will cause additional mismatches between them and capacitors of core array. Also, they need higher circuit complexity. In [15, 19, 20] some SAR ADC digital calibration technique with the dithering method have been proposed. The disadvantage of this technique is that, it is analyzed based on complicated mathematical calculations using matrix and inversing of them, therefore, its implementation require very complex circuit in digital calibration part.

In this work, a new SAR ADC digital calibration technique with offset injecting perturbation signal in digital domain is presented. In the proposed method, and in two steps, this offset will be injected in the two least significant capacitors in the basic capacitor array, separately. Also, sub radix-2 architecture [14, 17] is utilized in order to not to lose any code and prevent redundancy.

The advantages of this method is that: firstly, for applying the perturbation signal extra analog capacitor [15], which leads to new uncompensated mismatching between this analog capacitor and array capacitors, is not required. Secondly, comparing to preceding digital dithering method [16, 19, 20], it doesn't need complicated mathematical calculation. Thirdly, unlike split calibration, that requires two independent converters for production of two specified paths [17, 18], it just employs basic capacitor array which makes it possible with simple architecture.

This paper organizes the following chapters: in the second chapter a review on procedure of SAR ADS converters has been provided. In third chapter, calibration architecture and error correction procedure is introduced. In the fourth and fifth chapters simulation and conclusion are provided.

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2. Basic Principle of SAR

2.1 Binary SAR Architecture

In Fig. 1, a conventional form of SAR analog-to-digital converters has been showed. Commonly, it includes a DAC with binary weight therein each capacitor with more valuable weight is equal to total low-valuable capacitors. Analog input will be converted in N clock cycles to N-bit digital output. In first phase all capacitors are connected to input sample v_{in}, then capacitor c_{N-1} is connected to capacitor $+v_{ref}$ and the remaining capacitors connect to $-v_{ref}$. By redistribution of capacitor charges, total node voltage is obtained as below [10, 14, 17]:

$$v_{sum} = -v_{in} + {}^{c_{N-1}}/_{C_T} . v_{ref} - \frac{\sum_{i=0}^{N-2} c_i + c_0}{c_T} . v_{ref} \quad (1)$$

$$c_T = \sum_{i=0}^{N-1} c_i + c_0 \quad (2)$$

Considering v_{sum} sign, the comparer specifies d_{N-1} bit. If $V_{sum} > 0, d_{N-1}$ is zero and otherwise will be 1. This process is repeated in N clock pulse and for N bit:

$$v_{sum} = -v_{in} + \sum_{i=0}^{N-1} (2d_{i-1} - 1) \frac{c_i}{c_T} v_{ref} - \frac{c_0}{c_T} v_{ref} \quad (3)$$

In (3), it is observed that the share of each digital output bit is determined by a weight w_i that is equal to ${C_i}/{C_T}$. In ideal mode, the weights are equal to ${1}/{2^i}$ (i is the number of relative bit). In this mode, converter transfer curve is as linear function x=y [13].

Although binary algorithm is more efficient as respect to the conversion stages but is exposed to the analog disorders while implementing the actual circuit. Mismatch of capacitor in binary SAR ADC is static error resources (DNL, INL). For reducing these errors, often ADC including unit elements and capacitive divisions is used that is cause of circuits complexity in logic part such as binary to thermometry decoder circuit that ultimately results in speed drops of converter. In the mode of having error due to the mismatch of capacitors, the decision-making surfaces may not be distributed equally all over the input range. This distortion may lead in losing some codes, but that missing code maybe improved by digital calibration [13].

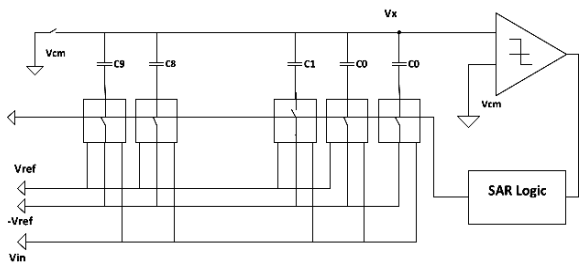


Fig. 1. SAR ADC structure

2.2 Sub Radix-2 Architecture DAC

If binary architecture without any modification is used, digital calibration cannot correct all types of mismatch errors. Fig. 2 illustrates several transfer curves for a 5-bit binary-scaled DAC [14]: Fig. 2a shows nominal curve, Fig. 2b shows curve in case of a positive DNL error in the MSB, and Fig. 2c shows curve in case of a negative DNL error in the MSB[14]. While considering the MSB only in this example, a comparable situation can occur with the other capacitors of the DAC. The large DNL error produced for DNL>0 cannot be reduced with calibration, as calibration can only re-map the input code to an existing combination of capacitors that approximates the desired output level. However, for DNL>0, there is no combination of capacitors available to fill the gap in the output range. On the other hand, the large DNL error for DNL<0 can be corrected with calibration, as there is a 'gap-free' consecutive of output levels. By digital re-mapping, the overlap of the curve can be removed to obtain a slick transfer curve. However, as a side effect of the overlap, the full-scale range of this converter will be slightly smaller than usual that is compensated by redundancy bit [13, 14].

Concisely, for the digital calibration to operate properly gaps (DNL>0) are not allowed but overlap (DNL<0) is allowed. By means of redundancy, the probability of a 'gap' can be reduced to an arbitrary low value by design: instead of designing the nominal transfer curve as in Fig. 2a (x=y), it is designed as in Fig. 2c. Thus, redundancy introduces intentional overlap (DNL<0) of the nominal transfer curve to guarantee that the consecutive of the output range remains, also in case of mismatch. While the figure illustrates redundancy for the MSB only, in reality this redundancy requirement needs to be implemented for each bit of the converter [13, 14, 17].

For the case that the more valuable weight is smaller than total capacitors, probably a code is lost.

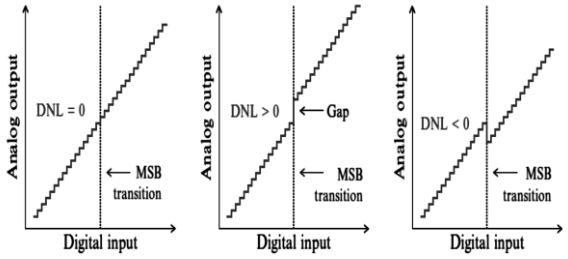


Fig. 2. Transfer curves for a 5-bit binary-scaled DAC:
left) Nominal curve middle) Curve case of a positive DNL error in the MSB right) Curve case of a negative DNL error in the MSB [14]

3. Calibration Method

Perturbation-based calibration algorithm has been introduced in [15]. In [15], perturbation signal in analog domain has been inserted to the inlet by two small capacitors. These capacitors increase the chip area. Furthermore, mismatch error between these inserted capacitors and the capacitors of SAR ADC cannot be compensated. Dithering method is used in [16], by applying a PN signal on the weights, the error is corrected by matrix and very complicated calculations which will lead to high amount of circuit a low speed in the

calibration unit. In this paper, the error has been compensated by adding two lower weights to the input.

In this paper a new structure of sub radix-2 algorithm has been used that reduces the complexity of circuit structure, in which by using the added weights w_0 and w_1 to the converter. Capacitor mismatch errors are corrected in digital domain.

Fig. 3 exhibits the first step of background calibration design of SAR ADC. As can be seen, to perturbation signal injection, the weight of lowest bit w_0 of the first stage is applied by V_{in}, in which the sum/subtract of these two makes the ADC input.

The operation is described as follows: a single SAR ADC digitizes each analog sample twice, with two offsets, where is the weight of lowest bit w_0. SAR ADC provides two outputs for each sample of analog input. D_+ is produced in lieu for input $V_{in} + w_0$ and D_- in lieu for $V_{in} - w_0$.

According to Fig. 3, the main output of ADC is produced out of the average of both outputs. The error is calculated by subtracting the outputs through reducing 2 w_0. So it can be written as:

$$\text{error} = \underbrace{\mathrm{D_+.W}}_{\mathrm{X_+}} - \underbrace{\mathrm{D_-.W}}_{\mathrm{X_-}} - 2\mathrm{w_0} \quad (4)$$

$$\mathrm{X_{out}} = \frac{\mathrm{X_+ + X_-}}{2} \quad (5)$$

where X_{out} is the final output of ADC.

Update equation of weights is obtained according to LMS method as following [15]:

$$\mathrm{w_i(n+1) = w_i(n) - \mu_w.error.(D_{+i}(n) - D_{-i}(n))} \quad (6)$$

Where μ_w is the convergence coefficient.

By this equation, all weights except w_0 will be updated and improved.

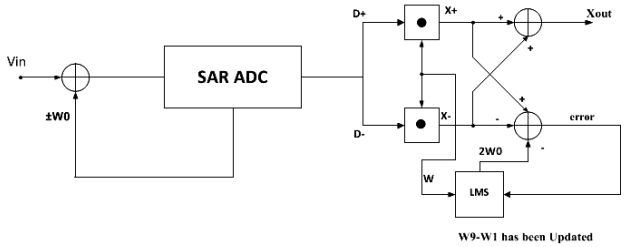


Fig. 3. Calibration diagram with injecting w0

In order to facilitate the signal injection of dither, as can be seen in the Fig. 4, the digital offset is injected through the lowest-valuable weight capacitor in capacitor banks of Fig. 1.

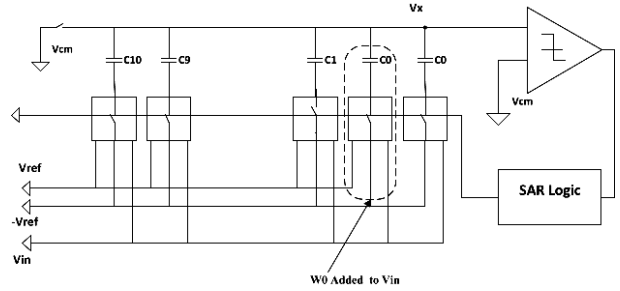


Fig. 4. Injecting w_0 to input

Adding and subtracting has been done by forward and reverse switching sequence of this capacitor, respectively [16]. So it can be said that:

$$\mathrm{V_{in} \pm w_0 = \sum_{i=1}^{N-1}(2b_i - 1)\,w_i + Q_e} \quad (7)$$

where V_{in} is the analog sample, Q_e is the quantization noise and w_i weight of the i'th bit.

In the second step calibration engine, and for updating w_0, the weight of $\pm w_1$ are added to V_{in} input (similar to w_0) and the error is obtained by calculating the difference of outputs and reducing $2w_1$ 2 as shown in Fig. 5 error is used to calibrate the weight of w_0 in terms of the following equation:

$$\text{error} = \underbrace{\mathrm{D_+.W}}_{\mathrm{X_+}} - \underbrace{\mathrm{D_-.W}}_{\mathrm{X_-}} - 2\mathrm{w_1} \quad (8)$$

and

$$\mathrm{w_0\,(n+1) = w_0(n) - \mu_w.error.(D_+(n) - D_-(n))} \quad (9)$$

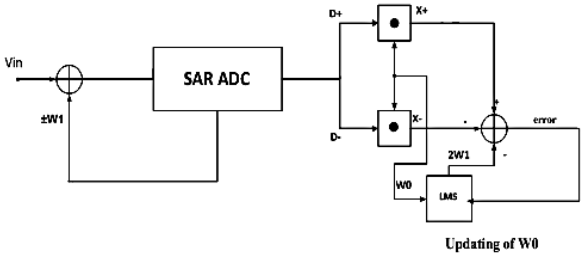


Fig. 5. Updating w_0 with injecting w_1

For the signal injection of second dither and for adding $\pm w_1$ to V_{in}, as can be seen in the Fig. 6 digital offset is injected through the second lowest-valuable weight capacitor in capacitor banks of Fig. 1(similar to preceding step). So it can be written as:

$$\mathrm{V_{in} \pm w_1 = w_0(2b_0 - 1) + \sum_{i-2}^{N-1}(2b_i - 1)w_i + Q_e} \quad (10)$$

Complete algorithm for the proposed calibration method is shown in Fig. 7. So it concluded that the proposed technique has several advantages: comparing with some preceding dithering method [15], for perturbation signal, this method does not use extra capacitor and employs same basic capacitor array. Furthermore, unlike [16,19,20], complicated mathematical and matrix calculation is not required. Also, unlike split calibration [17,18], double independent converters paths are not used.

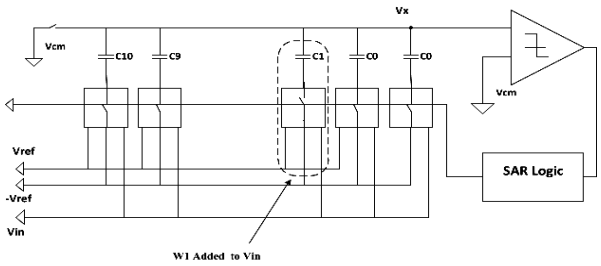


Fig. 6. Injecting w_1 to input

4. Simulation Results

A 10-bit SAR ADC has been simulated and calibrated by background digital calibration procedure and aiding MATLAB software. The capacity of capacitors in ADC has been specified according to sub radix-2 algorithm and mismatch 5% and with the base of 1.87, in accordance with first line of table I. The stability coefficients of LMS loop $\mu_w = 2^{-17}, \mu_e = 2^{-11}$ is chosen. INL and DNL diagrams before and after calibration modes are observed respectively in Fig. 8 and 9.

Fig. 8a and Fig. 8b show DNL diagrams and Fig. 9a and Fig. 9b show INL diagrams before and after calibration, respectively. In this figures the improvement of DNL and INL is completely evident. After calibration DNL and INL reduced from [-1, +12] LSB to [-0.1, +0.1] LSB and [-14.2, +14.2] LSB to [-0.34, +0.23] LSB, respectively. It should be pointed out that the effective number of bit is approximately is 10bit (which has maximum length of 2^{10}=1024 multiplied by LSB) and before calibration maximum length of DNL is about 14LSB. So DNL is less than 1.5% of maximum length in a 10bit converter. Upon reaching DNL to [-0.5, 0.5] LSB, missing code error is improved. Fig. 10 shows frequency response diagram before and after calibration. Static and dynamic specifications are shown in table II. After calibration, static and dynamic specifications have noticeable Improvement.

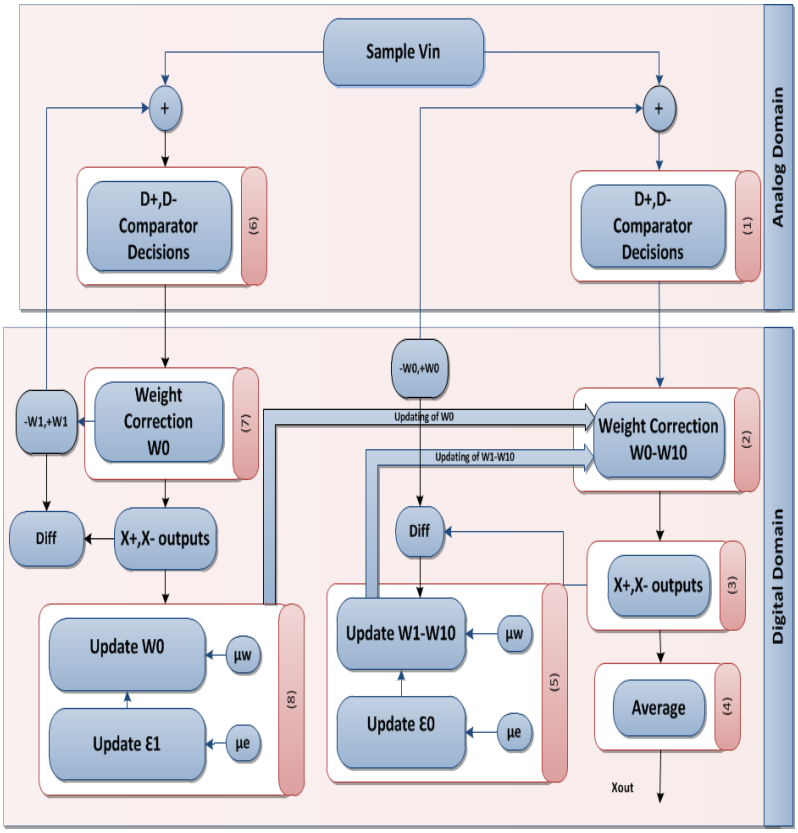
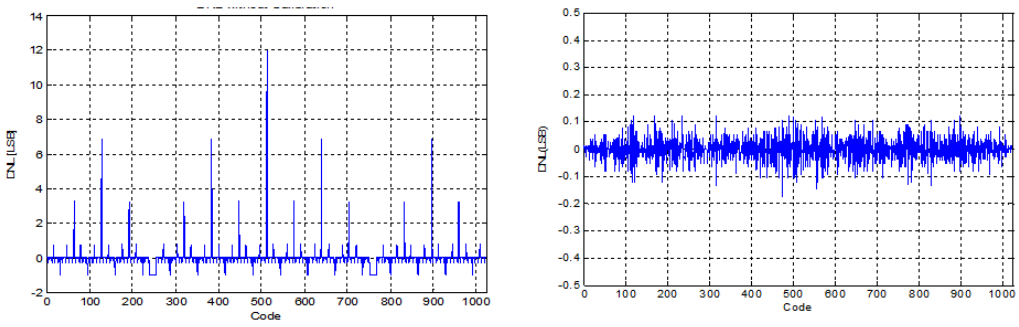
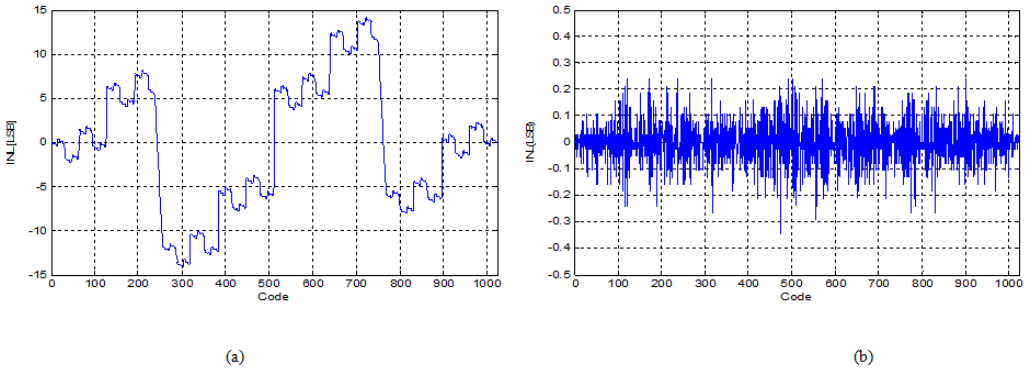


Fig. 7. Flowchart of calibration procedure



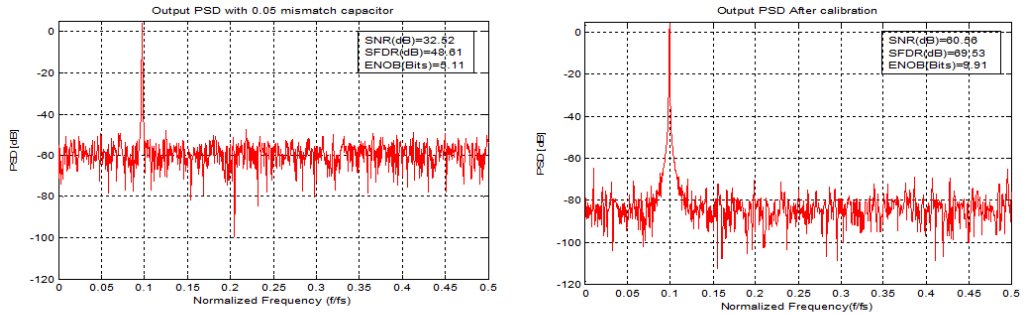
(a) (b)

Fig. 8. DNL Diagrams: a) Before calibration b) After calibration



(a) (b)

Fig. 9. INL Diagrams: a) Before calibration b) After calibration



(a) (b)

Fig. 10. Output PSD diagram: a) Before calibration b) After calibrat

Table 1. Static and dynamic specifications SAR ADC

	Before Calibration	After Calibration	Improvement Rate
DNL(LSB)	12	0.21	11.76
INL(LSB)	14.2	0.57	13.63
SNR (dB)	32.52	60.56	28.04
SFDR (dB)	48.61	69.53	20.92
ENOB (Bits)	5.11	9.91	4.8

5. Conclusion

A SAR ADC by digital background calibration method as well as sub radix-2 algorithm was presented. The dominant error in this converter was studied and improved by means of calibration method. Upon applying sub radix-2, no adaptation to the unit capacitor is required and it causes the simplicity of analog circuit and improvement of converter efficiency. Innovative result of this work is that perturbation signal is injected by the two least significant of existing elements in array capacitor of converter. So, this method does not need extra capacitor, so, related issue of mismatch between added element and existing elements in array capacitor will be eliminated. Furthermore, compared to the preceding works, it does not require complex mathematical calculations.

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